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FACULTY OF ENGINEERING & TECHNOLOGY

BCS-501 Operating System

Lecturer-24

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PAGING

- Implementation of Page Table
- Associative Memory
- Paging With TLB

Implementation of Page Table

•Page table is kept in main memory

•Page-table base register (PTBR) points to the page table

•Page-table length register (PTLR) indicates size of the page table

•In this scheme every data/instruction access requires two memory accesses

- •One for the page table and one for the data / instruction

•The two memory access problem can be solved by the use of a special fast-lookup hardware cache called associative memory or translation look-aside buffers (TLBs)

•Some TLBs store address-space identifiers (ASIDs) in each TLB entry – uniquely identifies each process to provide address-space protection for that process

- ➢Otherwise need to flush at every context switch

•TLBs typically small (64 to 1,024 entries)

•On a TLB miss, value is loaded into the TLB for faster access next time

- ➢Replacement policies must be considered
- ➢Some entries can be wired down for permanent fast access

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Associative Memory

•Associative memory – parallel search

Page #	Frame #

•Address translation (p, d)

- •If p is in associative register, get frame # out
- •Otherwise get frame # from page table in memory

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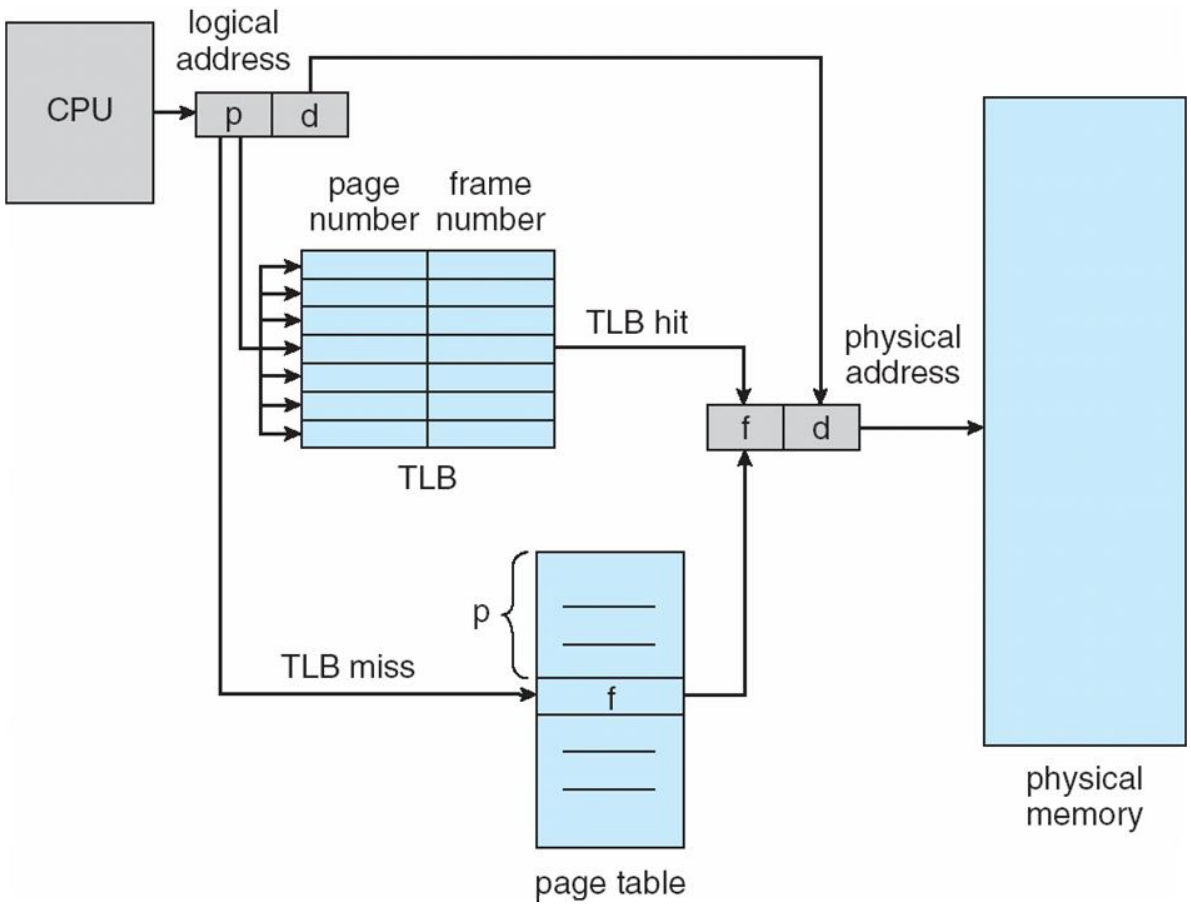
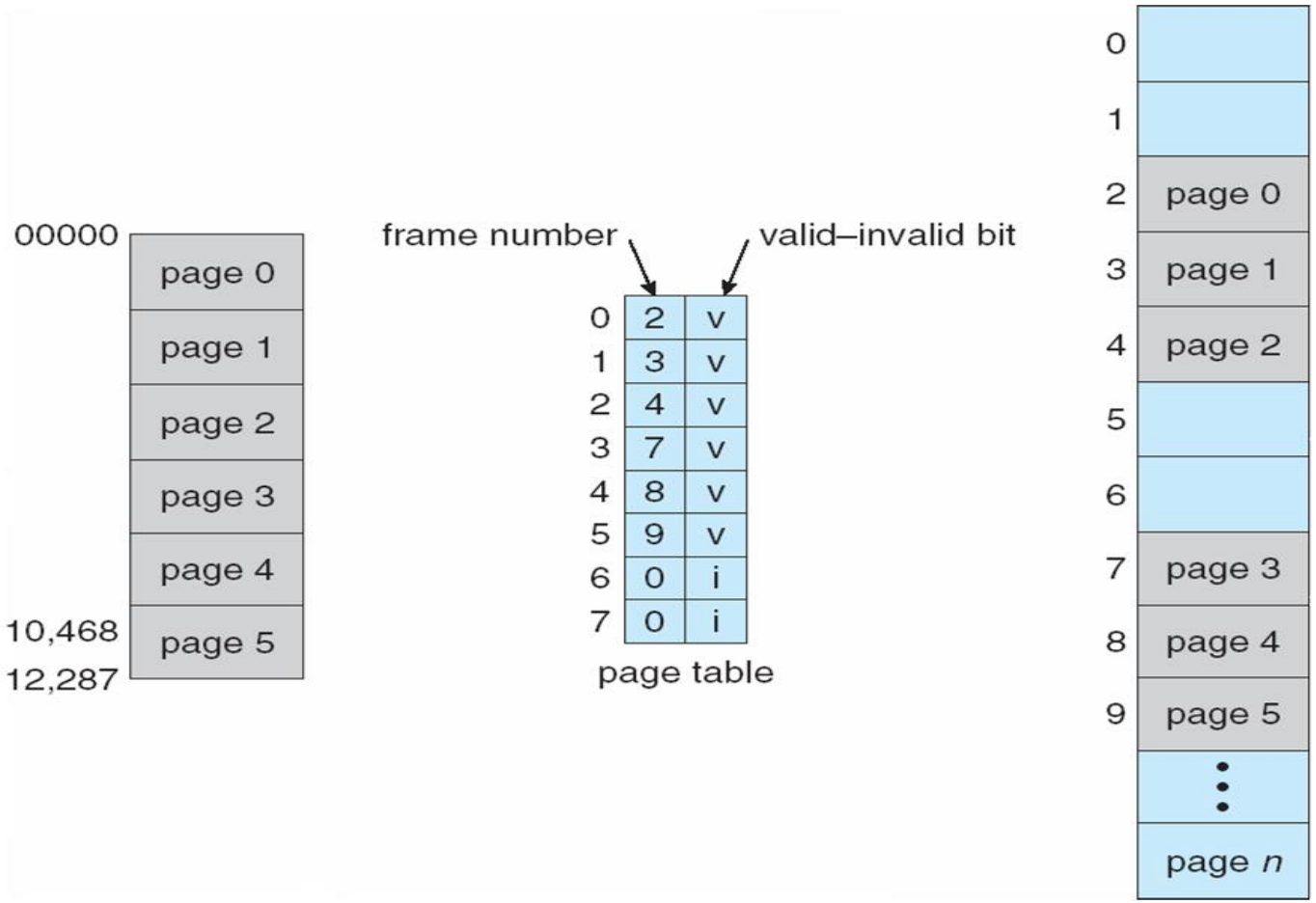
Paging With TLB



Page Table


00000
page 0
page 1
page 2
page 3
page 4
10,468
page 5
12,287
frame number
valid–invalid bit
0 2 v
1 3 v
2 4 v
3 7 v
4 8 v
5 9 v
6 0 i
7 0 i
page table
0
1
2 page 0
3 page 1
4 page 2
5
6
7 page 3
8 page 4
9 page 5
page n

MCQ

Which memory allocation policy allocate the largest hole to the process?
A. Best-Fit
B. Worst-Fit
C. First-Fit
D. None of them

When there is enough memory to fit a process in memory, but the space is not contiguous we need
A. Internal Fragmentation
B. Virtual Fragmentation
C. External Fragmentation
D. None of them

CPU fetches the instruction from memory according to the value of:
A. program counter
B. status register
C. instruction register
D. program status word

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Paging is implemented in

A. Operating System
B. Hardware
C. Software
D. All of them

Page-Table length register (PTLR) indicates size of

A. Page Table
B. Paging File
C. Main Memory
D. Virtual Memory

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